SESSION 22 – TAPA II
RF Circuit Techniques

Saturday, June 19, 8:00 a.m.
Chairpersons: P. Kinget, Columbia University
H. Sato, Renesas

22.1 — 8:00 a.m.
A 1.2 Volt 1.8GHz CMOS Quadrature Front-End, F. Tillman, N. Troedsson and H. Sjöland, Lund University, Lund, Sweden

A fully integrated 1.2V 0.25um CMOS quadrature front-end for a low or zero IF receiver has been designed and measured. The front-end consists of a common-gate LNA, a quadrature passive mixer, and a quadrature VCO operating at 1.8GHz. The conversion gain is 16dB, the noise figure is 6dB, the CP1 is -18dBm, the IIP2 is 27dBm, and the IIP3 is -6dBm. The total power consumption is 9.6mW and the IF quadrature phase error is below 1.8 degrees.

22.2 — 8:25 a.m.
A 15-GHz Integrated CMOS Switch with 21.5-dBm IP_{1dB} and 1.8-dB Insertion Loss, Z. Li and K.K. O, University of Florida, Gainesville, FL

A 15-GHz CMOS switch was fully integrated in a 0.13-mm CMOS foundry process. With on-chip LC impedance transformation networks, the switch achieves 21.5-dBm input P1dB and 34.5-dBm input IP3. The insertion loss and isolation are 1.8dB and 17.8dB. This is the first CMOS switch operating at 15 GHz with competitive performance as GaAs switches, and requires 3V/1.2V control voltages.

22.3 — 8:50 a.m.
A Circuit Technique Improving the Image Rejection of RF Front-Ends, S. Levantino, X. Wang*, P. Andreani*, C. Samori and A.L. Lacaita, Palitecnico di Milano, Milan, Italy, *Technical University of Denmark, Lyngby, Denmark

This work presents a technique to reduce the phase errors of quadrature signals. The proposed concept is demonstrated on a 2.4-GHz single-sideband up-converter in a 0.35μm BiCMOS process. The quadrature LO signals are obtained on-chip by means of two coupled oscillators, achieving a figure-of-merit of 186 dB. The image-rejection ratio improves by 7 to 11dB across the 28% LO tuning range with respect to a conventional design. The whole circuit dissipates 47mW.

22.4 — 9:15 a.m.
Low-power 5 GHz LNA and VCO in 90 nm RF CMOS, D. Linten, L. Aspemyr*, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Thijs, R. Garcia, H. Jacobsson*, P. Wambacq, S. Donnay and S. Decoutere., IMEC, Leuven, Belgium, *Ericsson AB, Molndal, Sweden

The potential of 90 nm CMOS technology for low-power RF front-ends is demonstrated with fully integrated low-voltage Low-Noise Amplifiers (LNA) andVoltage-Controlled Oscillators (VCO). The 5.5 GHz LNA draws 3.5 mA from a 0.6 V supply with a measured power gain of 11.2 dB, and a 3.2 dB noise figure. The 6.3 GHz VCO has a phase noise of –118 dBc/Hz at 1 MHz offset, drawing 4.9 mA from a 1.2 V supply.

22.5 — 9:40 a.m.
Accurate Subcircuit Model of an On-Chip Inductor with a New Substrate Network, M. Fujishima and J. Kino, The University of Tokyo, Chiba, Japan

The conventional inductor model has a measurable discrepancy in practice since the current flowing in a substrate is not correctly considered. In this paper, an accurate subcircuit model is proposed for an on-chip inductor with a new substrate network to consider losses generated in both vertical and horizontal directions. The proposed model gives an intelligent explanation of the reduction in equivalent resistance between terminals with increasing frequency. The simulation results show good agreement with the measurement over self-resonance frequency using the proposed inductor model.

Break 10:05 a.m.